Document Title

8M x 8 Bit NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue.	April 10th 1998	Preliminary
1.0	Data Sheet, 1998	July 14th 1998	Final
1.1	Data Sheet. 1999	April 10th 1999	Final
	1) Added $\overline{CE}$ dont care mode during the data-loading and reading		

8M x 8 Bit NAND Flash Memory

FEATURES

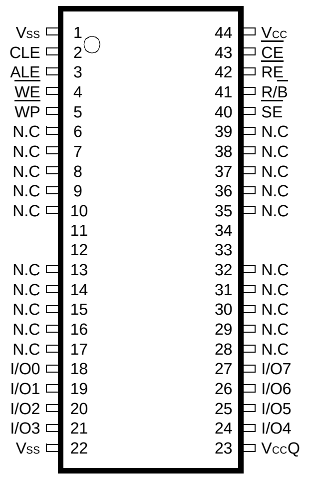
- Voltage Supply : 2.7V ~ 3.6V
- Organization
  - Memory Cell Array : (8M + 256K)bit x 8bit
  - Data Register : (512 + 16)bit x8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (8K + 256)Byte
- 528-Byte Page Read Operation
  - Random Access : 7µs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200µs(typ.)
  - Block Erase time : 2ms(typ.)
- Command/Address/Data Multiplexed I/O port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 1M Program/Erase Cycles
  - Data Retention : 10 years
- Command Register Operation
- 44(40) - Lead TSOP Type II (400mil / 0.8 mm pitch)

GENERAL DESCRIPTION

The KM29U64000 is a 8M(8,388,608)x8bit NAND Flash Memory with a spare 256K(262,144)x8bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typically 200µs and an erase operation can be performed in typically 2ms on an 8K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verify and margining of data. Even the write-intensive systems can take advantage of the KM29U64000′s extended reliability of 1,000,000 program/erase cycles by providing either ECC(Error Correcting Code) or real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications and also the spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC.

The KM29U64000 is an optimum solution for large nonvolatile storage applications such as solid state file storage, digital voice recorder, digital still camera and other portable applications requiring non-volatility.

PIN CONFIGURATION



44(40) TSOP (II)
STANDARD TYPE

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
$\overline{SE}$	Spare area Enable
R/$\overline{B}$	Ready/Busy output
Vcc	Power(2.7V ~ 3.6V)
VccQ	Output Buffer Power(2.7V~3.6V or 5.0V)
Vss	Ground
N.C	No Connection

NOTE : Connect all Vcc, VccQ and Vss pins of each device to power supply outputs.
Do not leave Vcc or Vss disconnected.

Figure 1. FUNCTIONAL BLOCK DIAGRAM

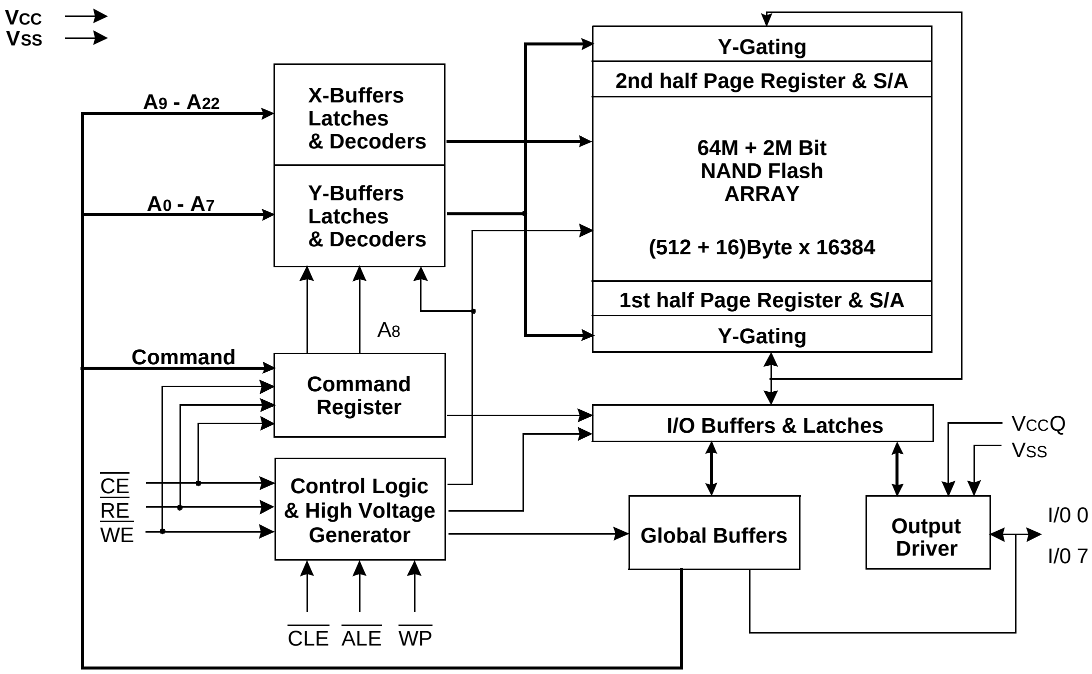
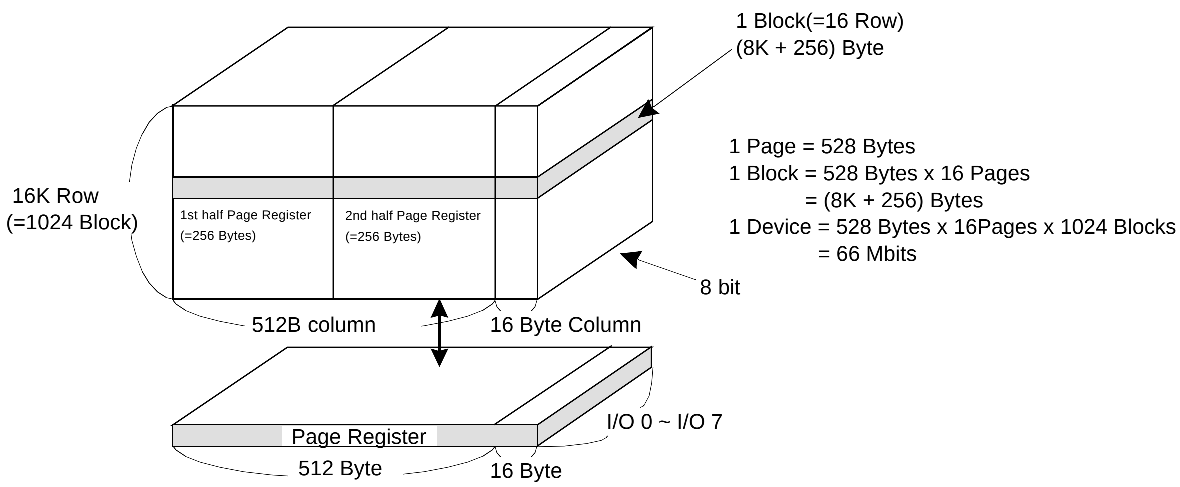


Figure 2. ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	*X	*X	**(Page Address)**

NOTE : Column Address : Starting Address of the Register.

00h Command(Read) : Defines the starting address of the 1st half of the register.

01h Command(Read) : Defines the starting address of the 2nd half of the register.

* A_8 is internally set to "Low" or "High" by the 00h or 01h Command.

* X can be High or Low.

PRODUCT INTRODUCTION

The KM29U64000 is a 66Mbit(69,206,016 bit) memory organized as 16,384 rows by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 16 pages formed by one NAND structures, totaling 4,224 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1024 separately erasable 8K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the KM29U64000.

The KM29U64000 has addresses multiplexed into 8 I/O′s. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: one cycle for erase-setup and another for erase-execution after block address loading. The 8M byte physical space requires 23 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used.
Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the KM29U64000.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Sequential Data Input	80h	-	
Read 1	00h/01h(1)	-	
Read 2	50h(2)	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	10h	-	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE : 1. The 00H command defines starting address of the 1st half of registers.
The 01H command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.
2. The 50h command is valid only when the $\overline{SE}$(pin 40) is low level.

PIN DESCRIPTION

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable(ALE)

The ALE input controls the path activation for address and input data to the internal address/data register.
Addresses are latched on the rising edge of $\overline{WE}$ with ALE high, and input data is latched when ALE is low.

Chip Enable($\overline{CE}$)

The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.

Write Enable($\overline{WE}$)

The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.

Read Enable($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.

Spare Area Enable($\overline{SE}$)

The $\overline{SE}$ input controls the spare area selection when $\overline{SE}$ is high, the device is deselected the spare area during Read1, Sequential data input and Page Program.

I/O Port : I/O 0 ~ I/O 7

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.

Write Protect($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready/$\overline{Busy}$(R/$\overline{B}$)

The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

Power Line(VCC & VCCQ)

The VCCQ is the power supply for I/O interface logic. It is electrically isolated from main power line(VCC=2.7V~3.6V) for supporting 5V tolerant I/O with 5V power supply at VCCQ.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{IN}	-0.6 to + 6.0	V
		V_{CC}	-0.6 to + 4.6	V
		$V_{CC}Q$	-0.6 to + 6.0	V
Temperature Under Bias	KM29U64000T	T_{BIAS}	-10 to + 125	°C
	KM29U64000IT		-40 to + 125	
Storage Temperature		T_{STG}	-65 to + 150	°C
Short Circuit Output Current		I_{OS}	5	mA

NOTE :
1. Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is $V_{CC}Q$+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, KM29U64000T:T_A=0 to 70°C, KM29U64000IT:T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	$V_{CC}Q^{*1}$	2.7	-	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

NOTE :
1. V_{CC} and $V_{CC}Q$ pins are separated each other.

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	$I_{CC}1$	tcycle=50ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	10	20	mA
	Program	$I_{CC}2$	-	-	10	20	
	Erase	$I_{CC}3$	-	-	10	20	
Stand-by Current(TTL)		$I_{SB}1$	$\overline{CE}$=V_{IH}, $\overline{WP}$=$\overline{SE}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		$I_{SB}2$	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=$\overline{SE}$=0V/V_{CC}	-	10	50	μA
Input Leakage Current		I_{LI}	V_{IN}=0 to 3.6V	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to 3.6V	-	-	±10	
Input High Voltage		V_{IH}	I/O pins	2.0	-	$V_{CC}Q$+0.3	V
			Except I/O pins	2.0	-	V_{CC}+0.3	
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	I_{OH}=-400μA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1014	1020	1024	Blocks

NOTE :
1. The KM29U64000 may include invalid blocks. Invalid blocks are defined as blocks that contain one or more bad bits. Do not try to access these invalid blocks for program and erase. During its lifetime of 10 years and/or 1million program/erase cycles,the minimum number of valid blocks are guaranteed though its initial number could be reduced. (Refer to the attached technical notes)
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block

AC TEST CONDITION

(KM29U64000T:T_A=0 to 70°C, KM29U64000IT:T_A=-40 to 85°C, V_{CC}=2.7V~3.6V unless otherwise noted)

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load (3.0V +/-10%)	1 TTL GATE and CL = 50pF
Output Load (3.3V +/-10%)	1 TTL GATE and CL = 100pF

CAPACITANCE(T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{SE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	X	Read Mode	Command Input
L	H	L	↑	H	X	X		Address Input(3clock)
H	L	L	↑	H	X	H	Write Mode	Command Input
L	H	L	↑	H	X	H		Address Input(3clock)
L	L	L	↑	H	L/H(3)	H	Data Input	
L	L	L	H	↓	L/H(3)	X	Sequential Read & Data Output	
L	L	L	H	H	L/H(3)	X	During Read(Busy)	
X	X	X	X	X	L/H(3)	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
3. When $\overline{SE}$ is high, spare area is deselected.

Program/Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	200	1000	µs
Number of Partial Program Cycles in the Same Page	Nop	-	-	10	cycles
Block Erase Time	t_{BERS}	-	2	4	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	50	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	7	µs
ALE to $\overline{RE}$ Delay(ID read)	t_{AR1}	100	-	ns
ALE to $\overline{RE}$ Delay(Read cycle)	t_{AR2}	50	-	ns
$\overline{CE}$ to $\overline{RE}$ Delay(ID read)	t_{CR}	100	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	30	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	15	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
Last RE High to Busy(at sequential read)	t_{RB}	-	100	ns
$\overline{CE}$ High to Ready(in case of interception by $\overline{CE}$ at read)(1)	t_{CRY}	-	50 +tr(R/$\overline{B}$)(2)	ns
$\overline{CE}$ High Hold Time(at the last serial read)(3)	t_{CEH}	100	-	ns
$\overline{RE}$ Low to Status Output	t_{RSTO}	-	35	ns
$\overline{CE}$ Low to Status Output	t_{CSTO}	-	45	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
$\overline{RE}$ access time(Read ID)	t_{READID}	-	35	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500	µs

NOTE : 1. If $\overline{CE}$ goes high within 30ns after the rising edge of the last $\overline{RE}$, R/$\overline{B}$ will not return to V_{OL}.
2. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.
3. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. Typically, an invalid block will contain a single bad bit. The information regarding the invalid block(s) is so called as the invalid block information. The invalid block information is written to the 1st or the 2nd page of the invalid block(s) with 00h data. Devices with invalid block(s) have the same quality level or as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block of the NAND Flash, however, is fully guaranteed to be a valid block.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block information is written prior to shipping. **Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 1). Any intentional erasure of the original invalid block information is prohibited.**

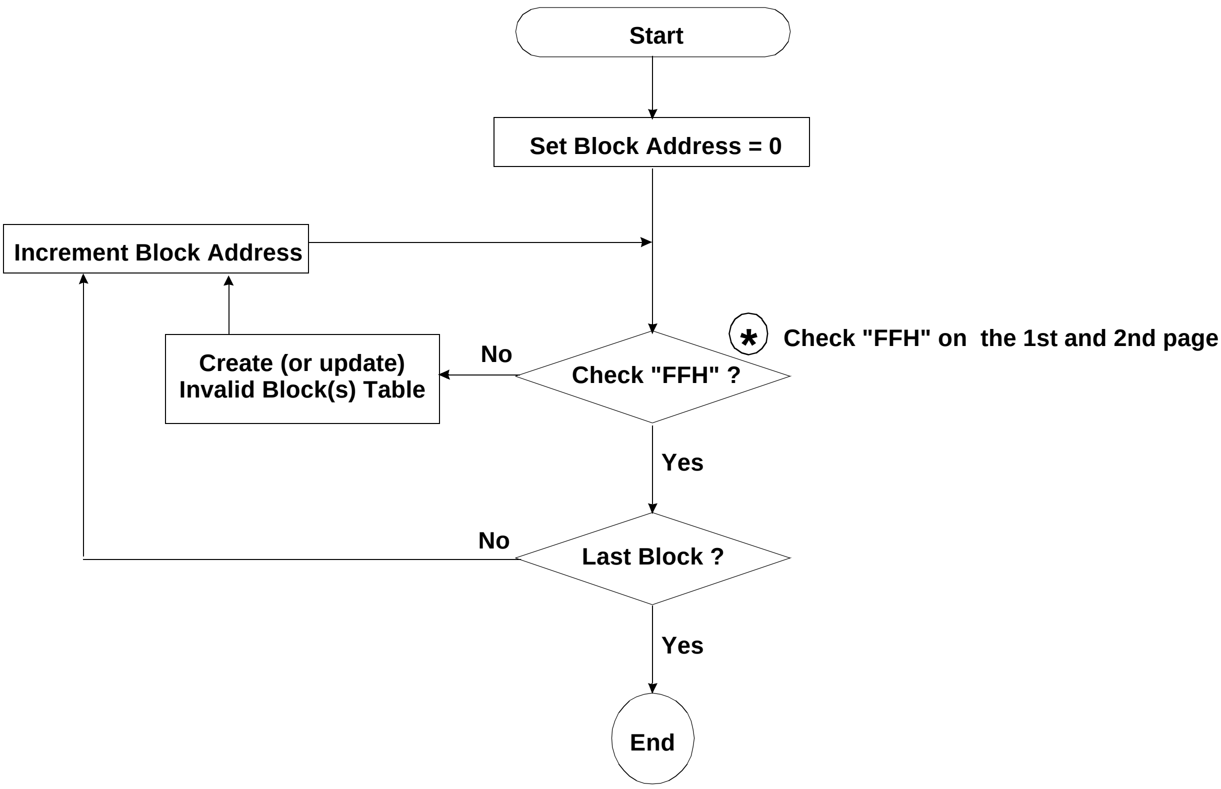


Figure 1. Flow chart to create invalid block table.

NAND Flash Technical Notes (Continued)

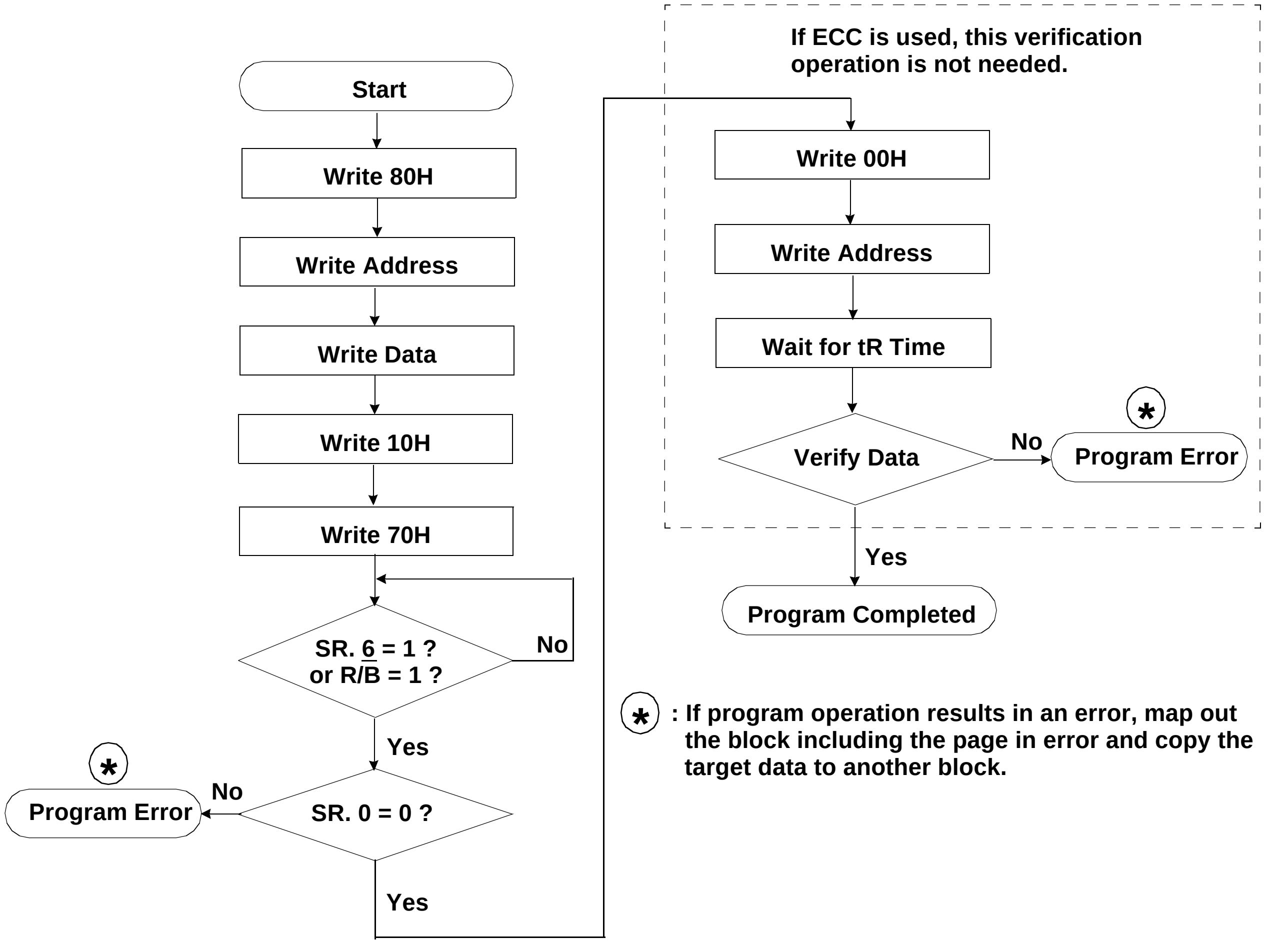
Error in write or read operation

Over its life time, the additional invalid blocks may occur. Through the tight process control and intensive testing, Samsung minimizes the additional block failure rate, which is projected below 0.1% up until 1million program/erase cycles. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> Block Replacement or ECC Correction

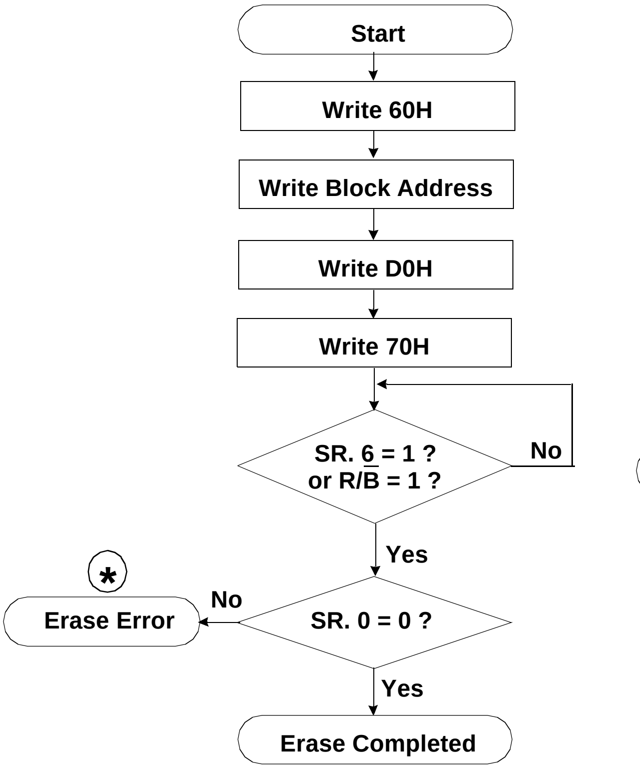
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart



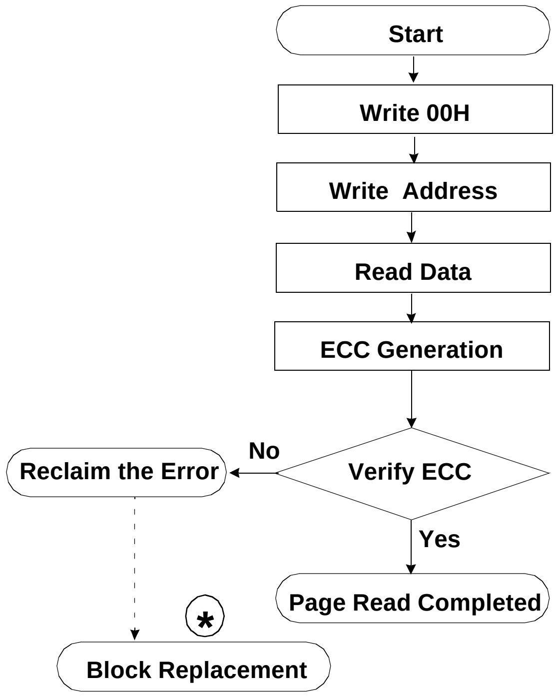
NAND Flash Technical Notes (Continued)

Erase Flow Chart



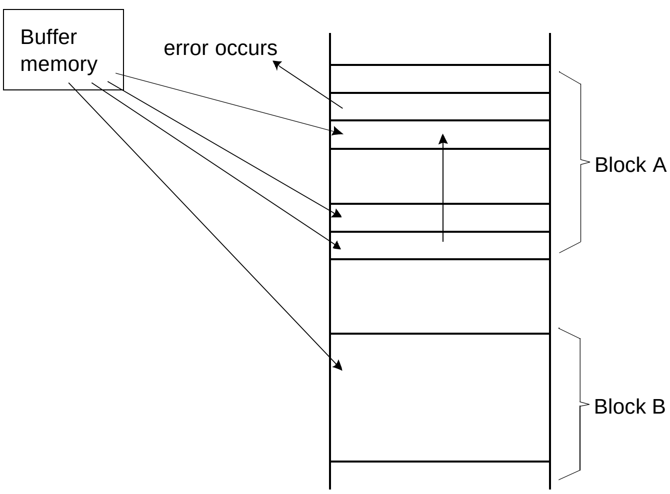
* : If erase operation results in an error, map out the failing block and replace it with another block.

Read Flow Chart



* : copy the corrected whole block data to another block (recommended for high reliability system)

Block Replacement



When the error happens in Block "A", try to write the data into another Block "B" by reloading from an external buffer. Then, prevent further system access to Block "A"(by creating a "invalid block" table or other appropriate scheme.)

Pointer Operation of KM29U64000

The KM29U64000 has three read modes to set the destination of the pointer. The pointer is set to "A" area by the "00h" command, to "B" area by the "01" command, and to "C" area by the "50h" command. Table 1 shows the destination of the pointer, and figure 2 shows the block diagram of its operations.

Table 1. Destination of the pointer

Command	Pointer position	Area
00H	0 ~ 255 byte	1st half array(A)
01H	256 ~ 511 byte	2nd half array(B)
50H	512 ~ 527 byte	spare array(C)

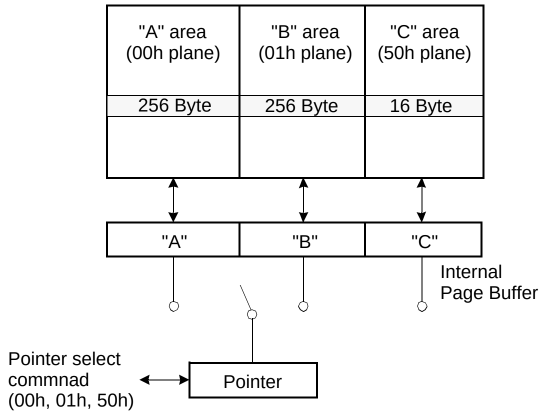
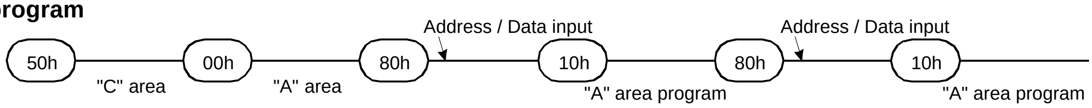


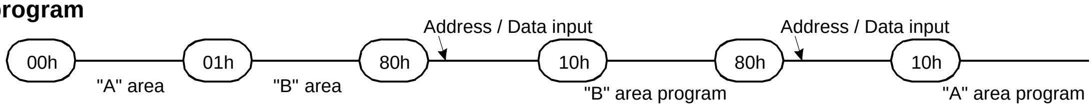
Figure 2. Block diagram of pointer Operation

Example of Pointer Operation programming

(1) "A" area program



(2) "B" area program



(3) "C" area program

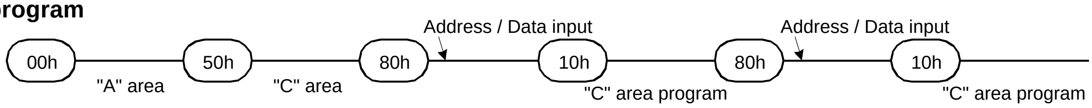


Table 2. Pointer Status after each operation

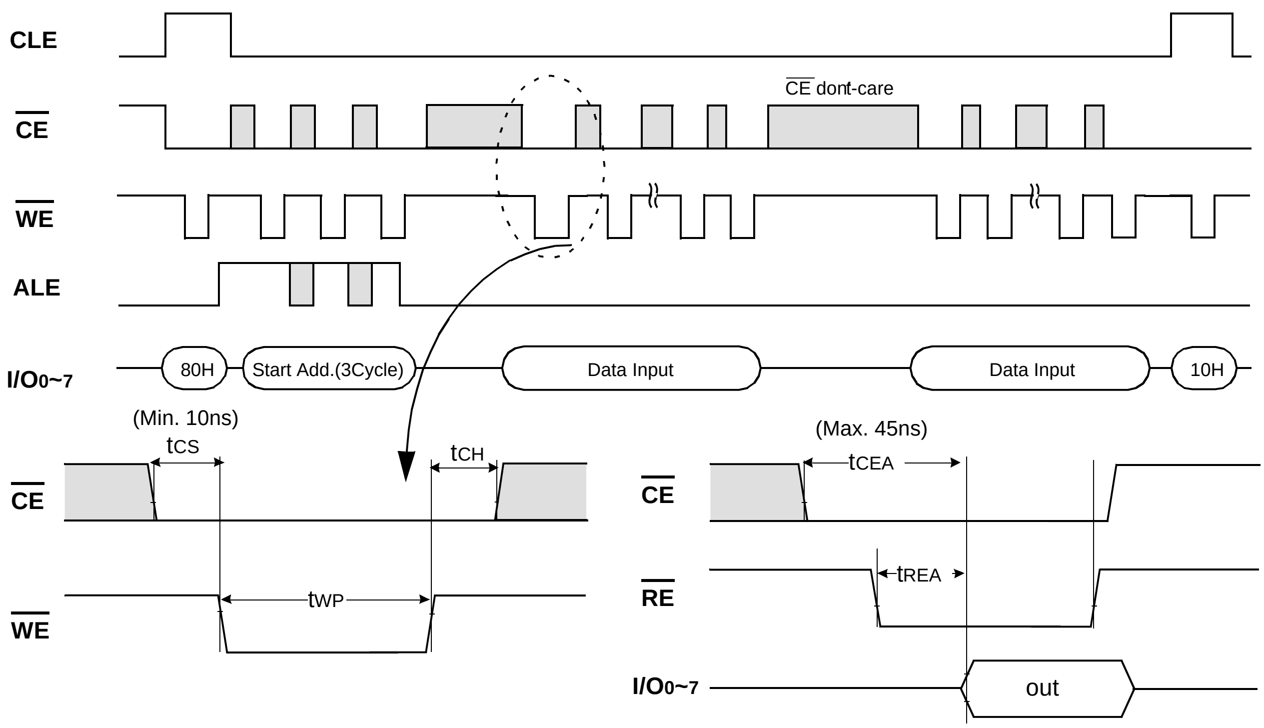
Operation	Pointer status after operation
Program/Erase	With previous 00H, Device is set to 00H Plane With previous 01H, Device is set to 00H Plane* With previous 50H, Device is set to 50H Plane
Reset	"00h" Plane("A" area)
Power up	"00h" Plane("A" area)

* 01H command is valid just one time when it is used as a pointer for program/erase.

System Interface Using $\overline{CE}$ dont-care.

For a easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

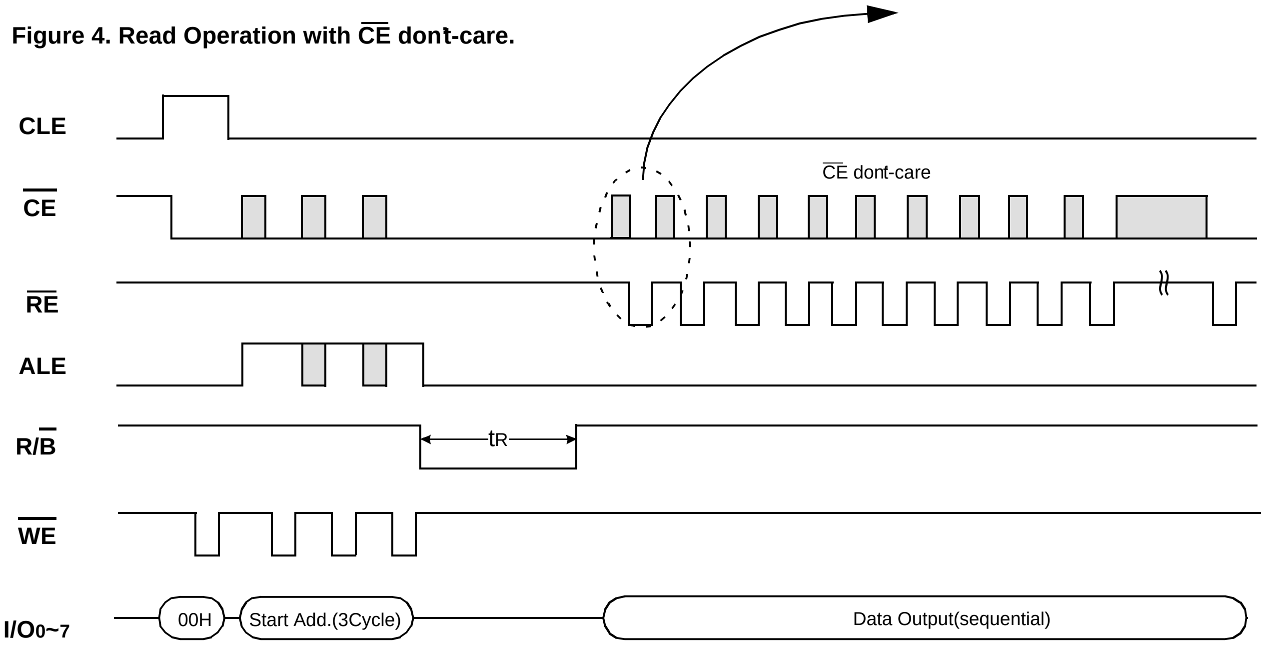
Figure 3. Program Operation with $\overline{CE}$ dont-care.



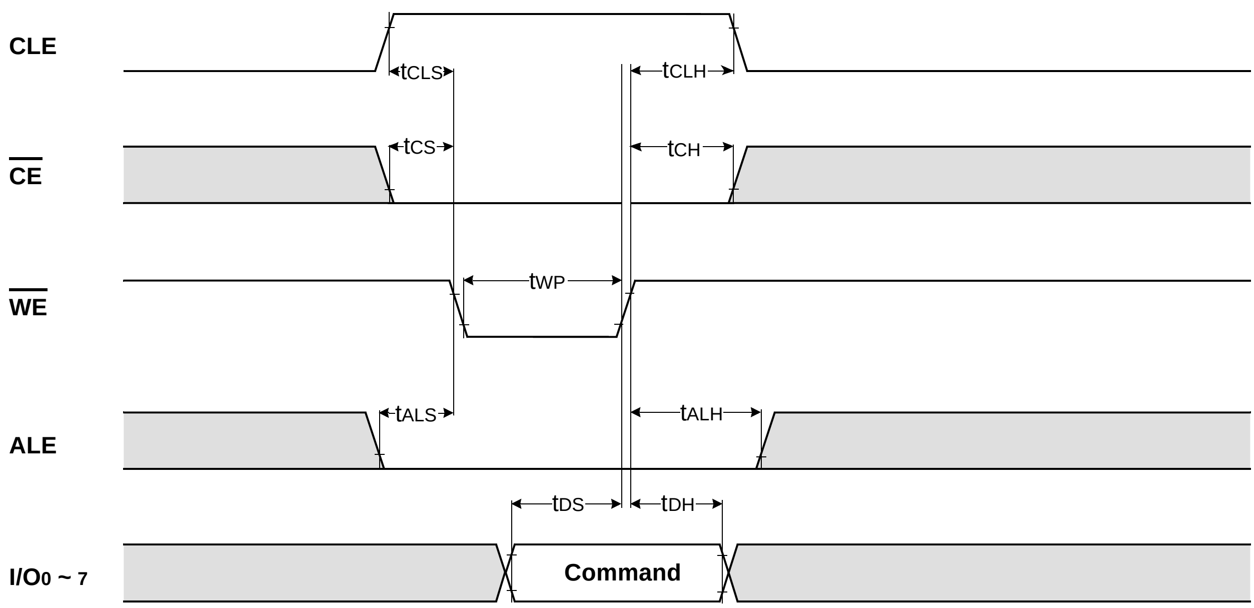
Timing requirements : If $\overline{CE}$ is is exerted high during data-loading, tCS must be minimum 10ns and tWC must be increased accordingly.

Timing requirements : If $\overline{CE}$ is is exerted high during sequential data-reading, the falling edge of $\overline{CE}$ to valid data(tCEA) must be kept greater than 45ns.

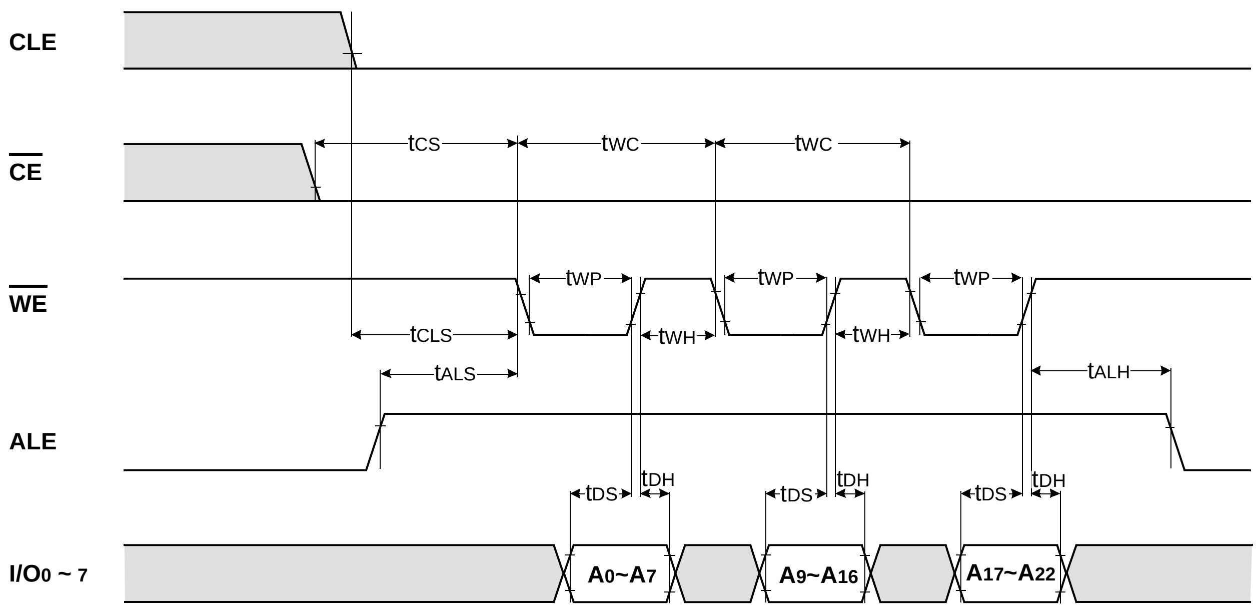
Figure 4. Read Operation with $\overline{CE}$ dont-care.



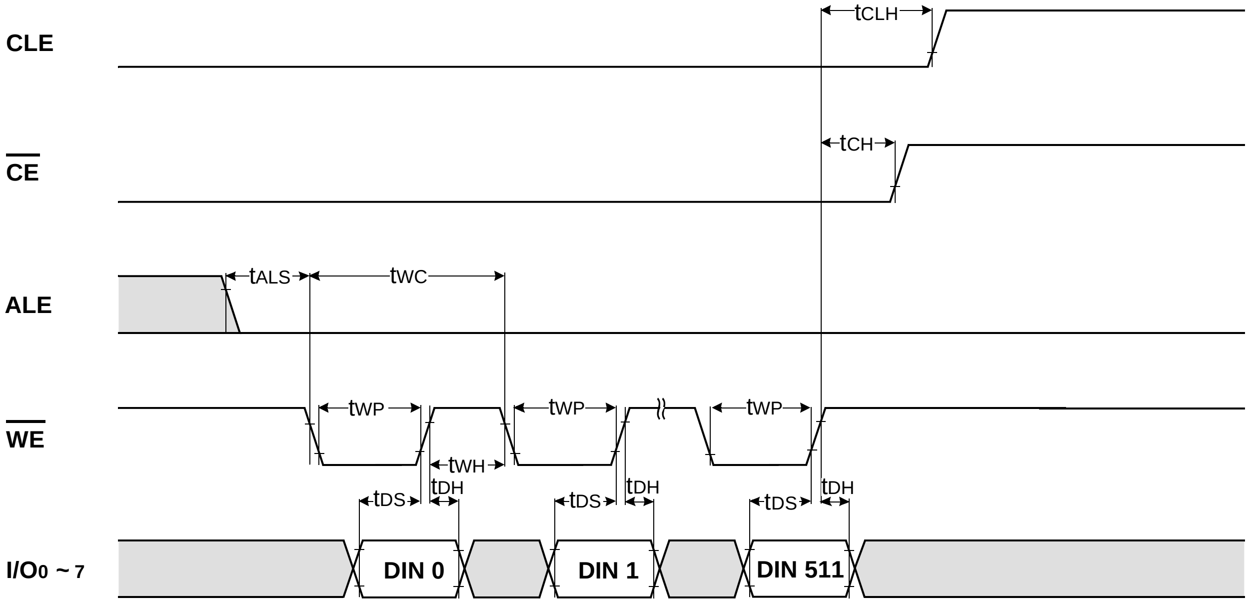
*** Command Latch Cycle**



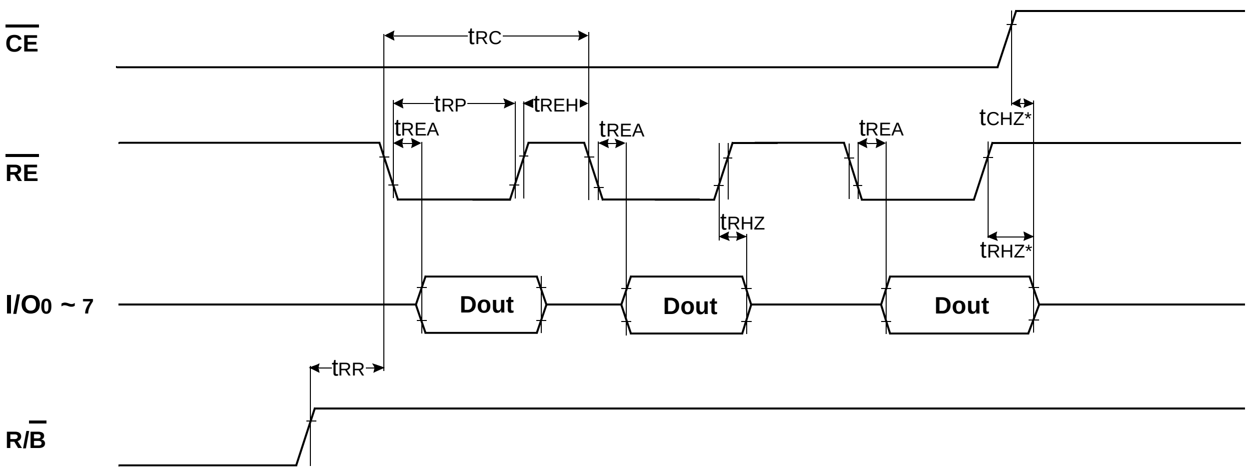
*** Address Latch Cycle**



* Input Data Latch Cycle

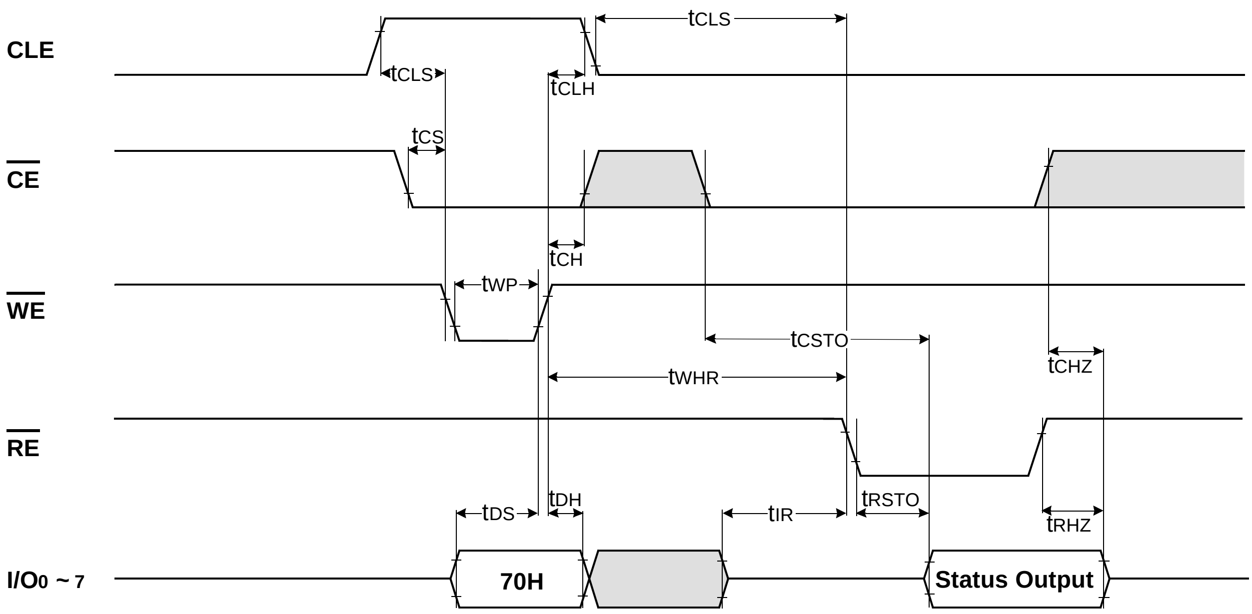


* Sequential Out Cycle after Read(CLE=L, WE=H, ALE=L)

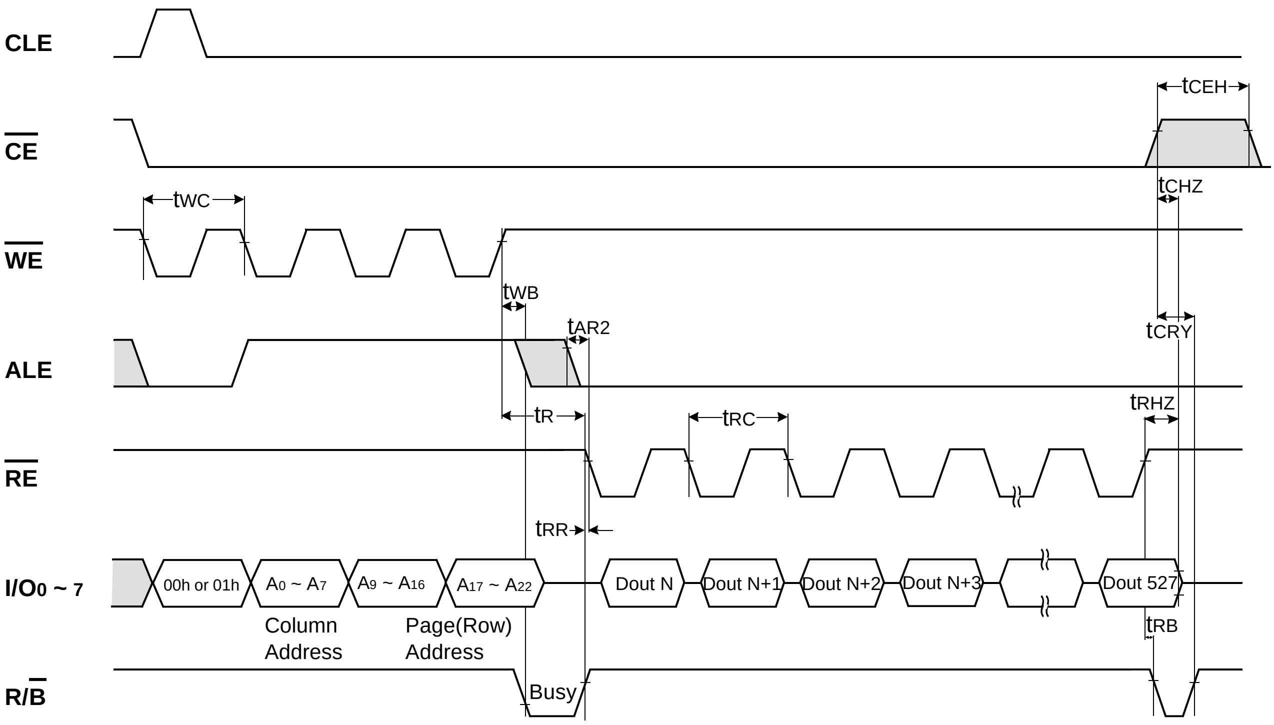


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

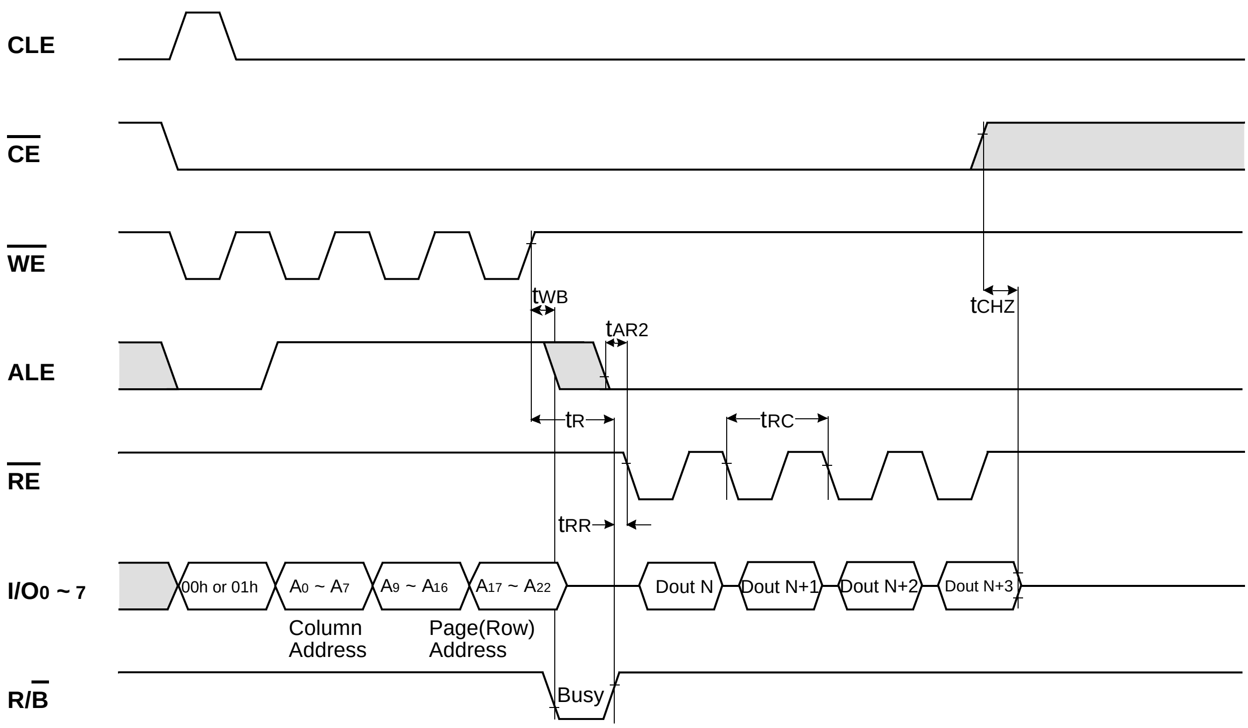
* Status Read Cycle



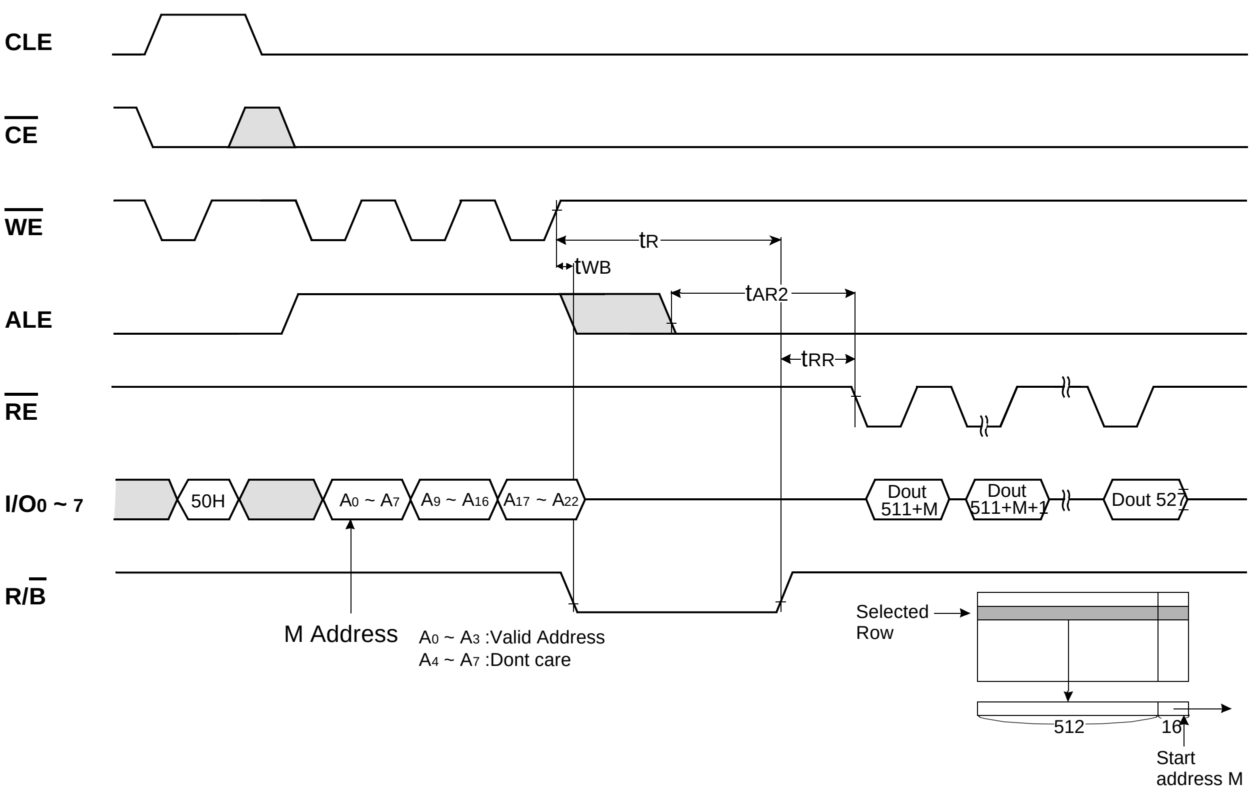
READ1 OPERATION(READ ONE PAGE)



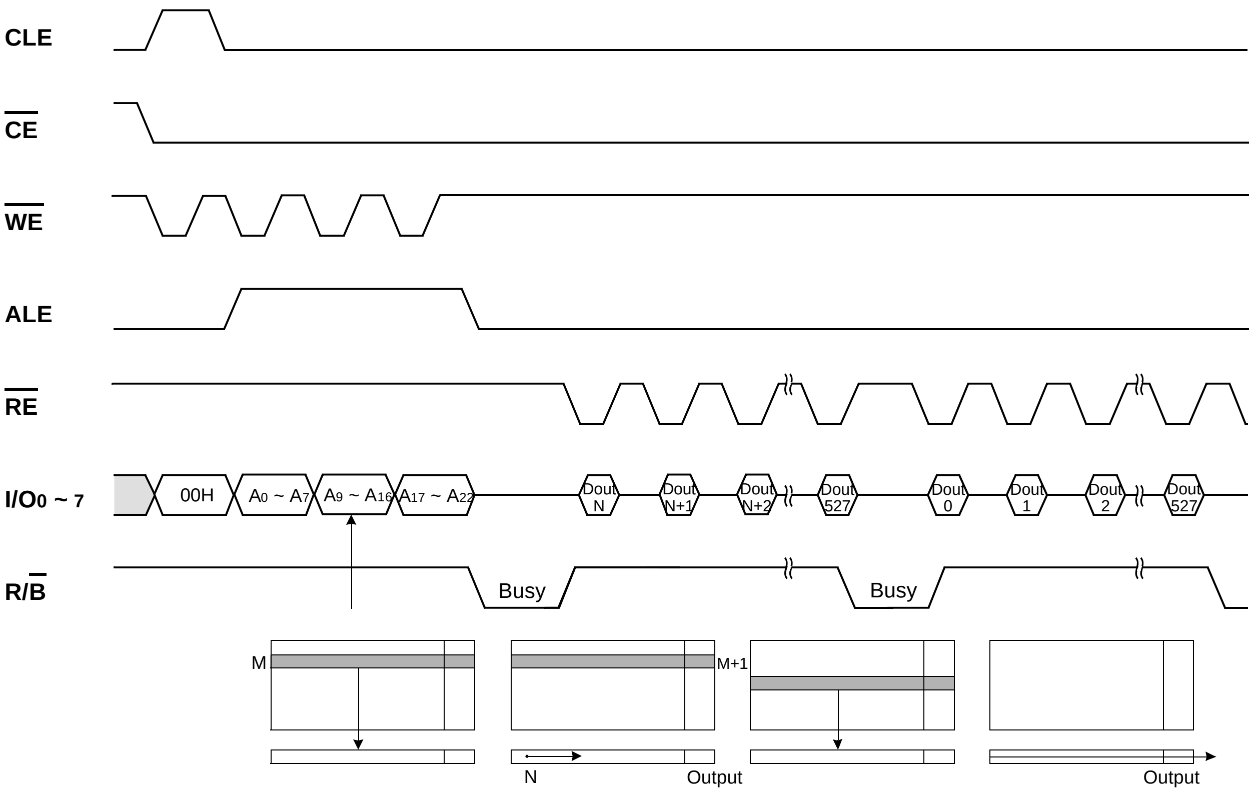
READ1 OPERATION(INTERCEPTED BY $\overline{CE}$)



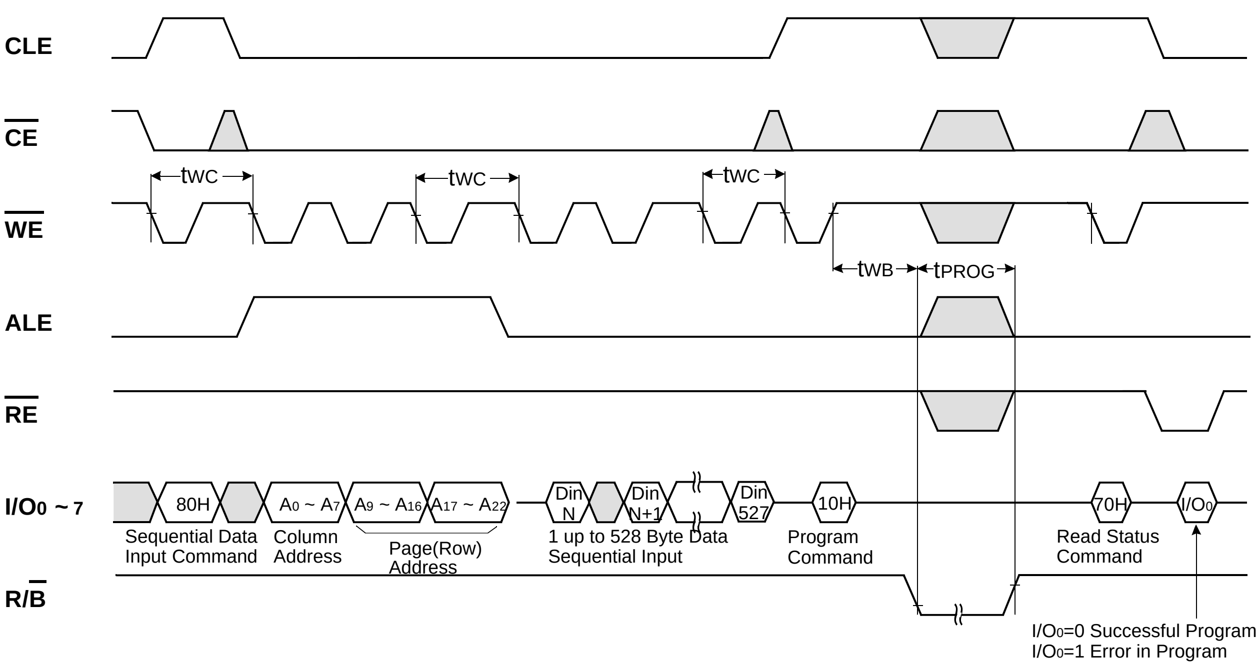
READ2 OPERATION(READ ONE PAGE)



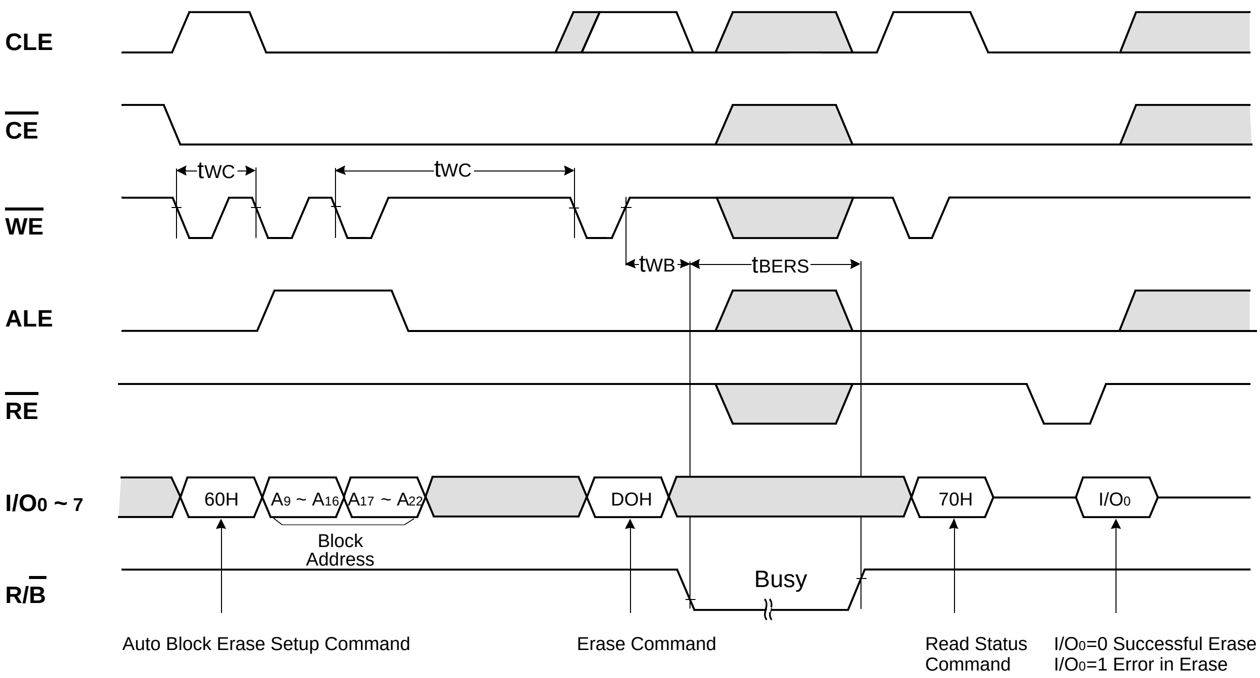
SEQUENTIAL ROW READ OPERATION



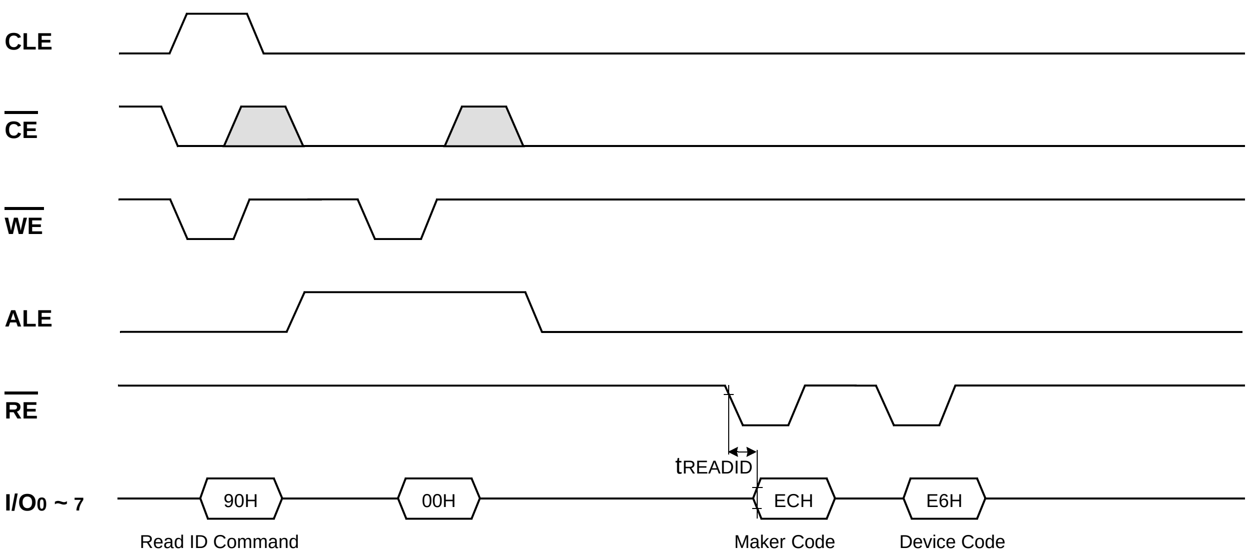
PAGE PROGRAM OPERATION



BLOCK ERASE OPERATION(ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION

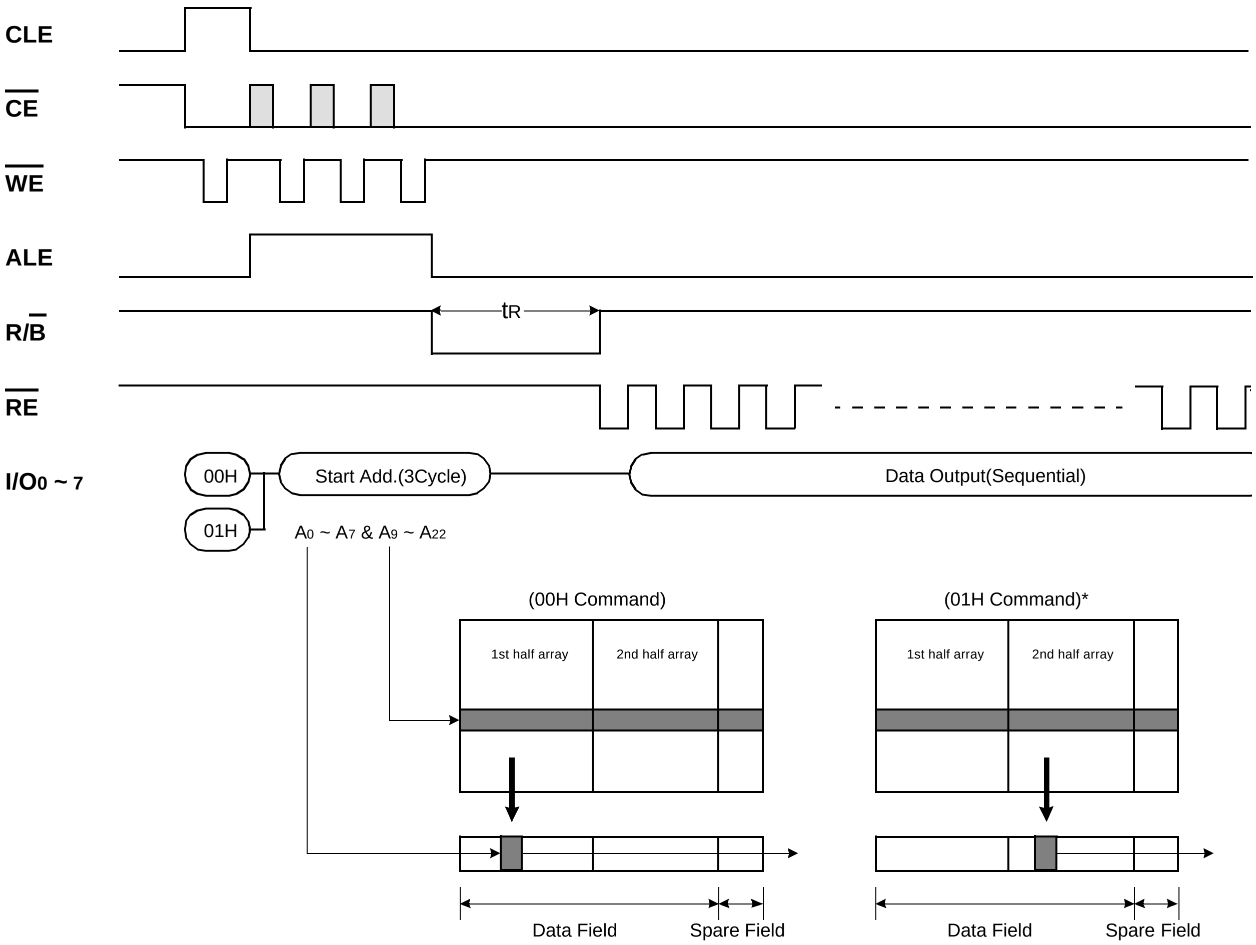


DEVICE OPERATION

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00H to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read.
The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 7µs(tR). The CPU can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE. High to low transitions of the RE clock output the data stating from the selected column address up to the last column address(column 511 or 527 depending on the state of SE pin).
After the data of last column address is clocked out, the next page is automatically selected for sequential row read.
Waiting 7µs again allows reading the selected page.The sequential row read operation is terminated by bringing CE high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command with SE pin low. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00H/01H) is needed to move the pointer back to the main area. Figures 3 thru 6 show typical sequence and timings for each read operation.

Figure 3. Read1 Operation



* After data access on 2nd half array by 01H command, the start pointer is automatically moved to 1st half array (00H) at next cycle.

Figure 4. Read2 Operation

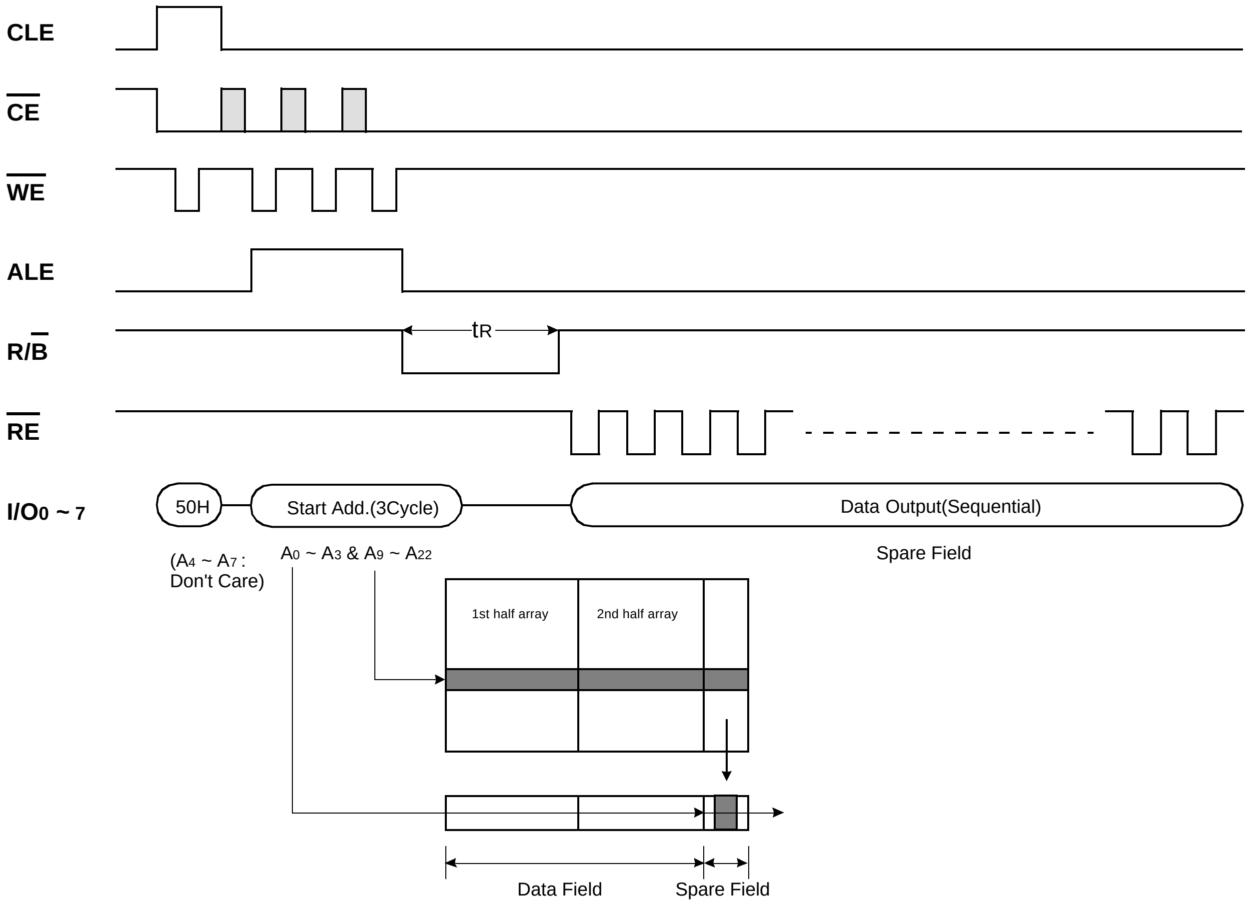


Figure 5. Sequential Row Read1 Operation

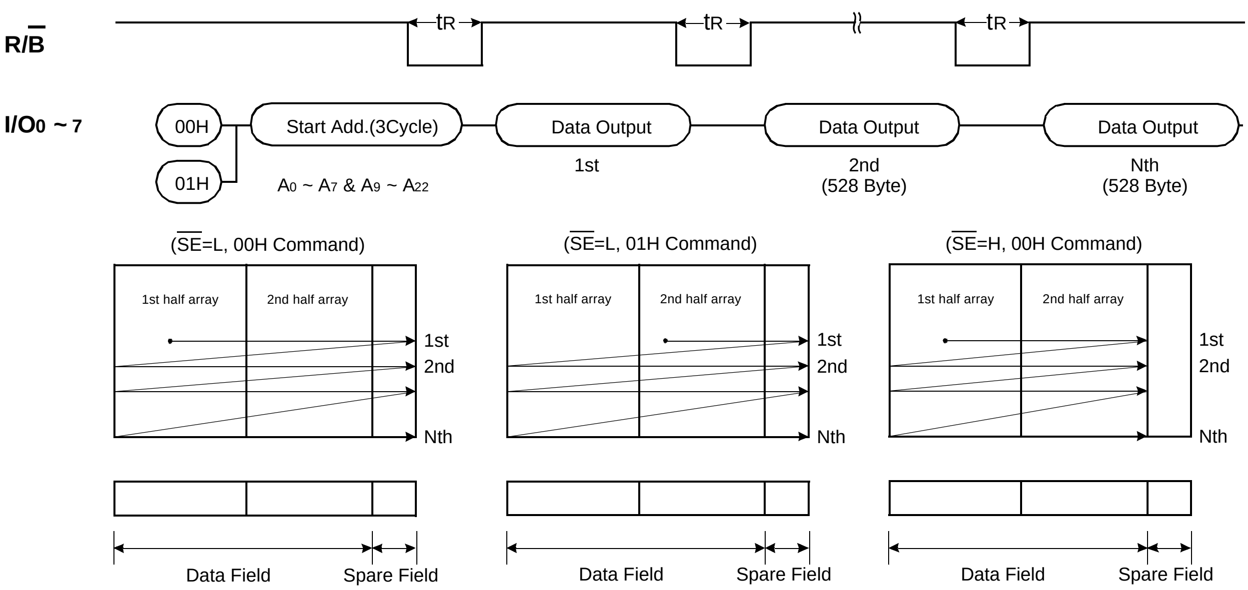
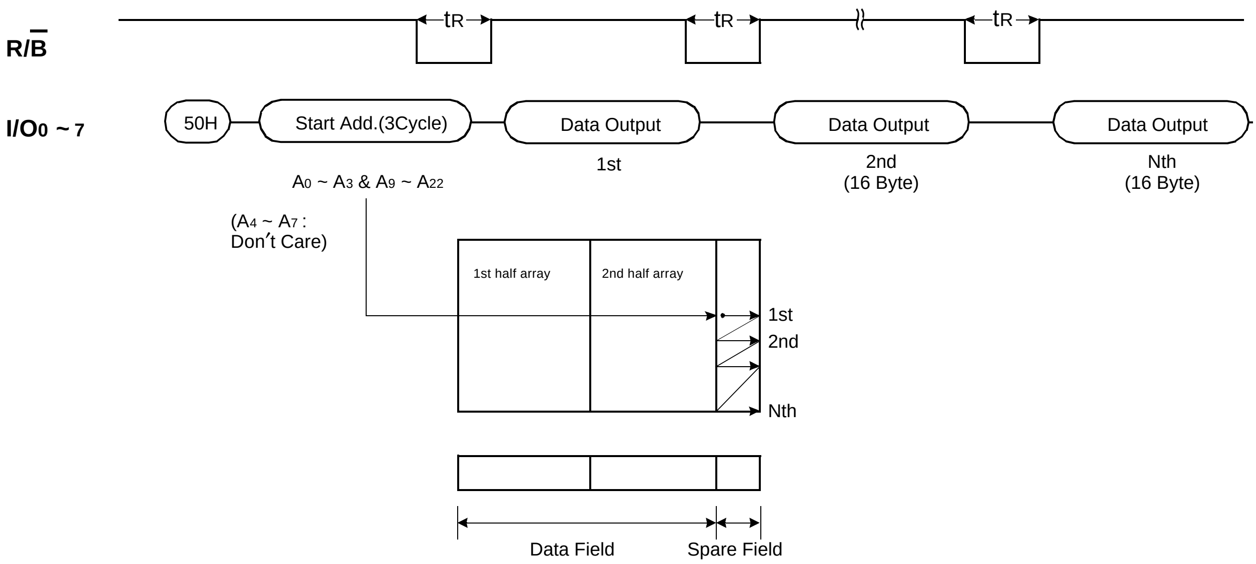


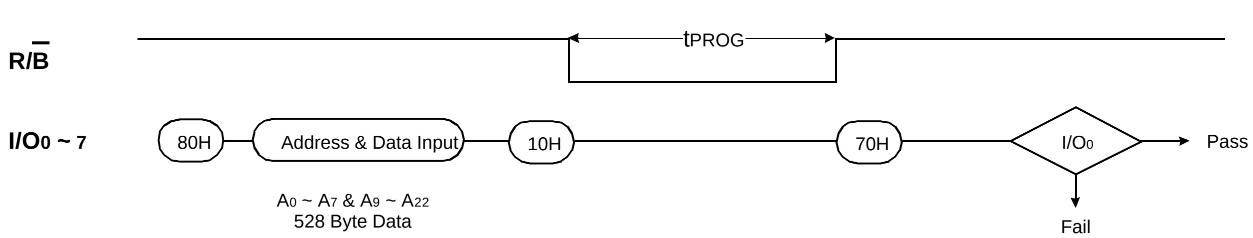
Figure 6. Sequential Row Read2 Operation(SE=fixed low)



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed ten. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.
The serial data loading period begins by inputting the Serial Data Input command(80H), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10H) initiates the programming process. Writing 10H alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with RE and CE low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 7). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

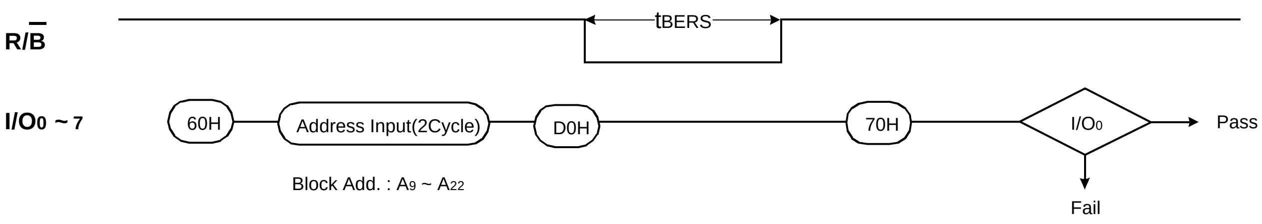
Figure 7. Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(8K Byte) basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60H). Only address A_{13} to A_{22} is valid while A_9 to A_{12} is ignored. The Erase Confirm command(D0H) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE after the erase confirm command input, the internal write controller handles erase, erase-verify and pulse repetition where required. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked.
Figure 8 details the sequence.

Figure 8. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70H command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00H or 50H) should be given before sequential page read cycle.

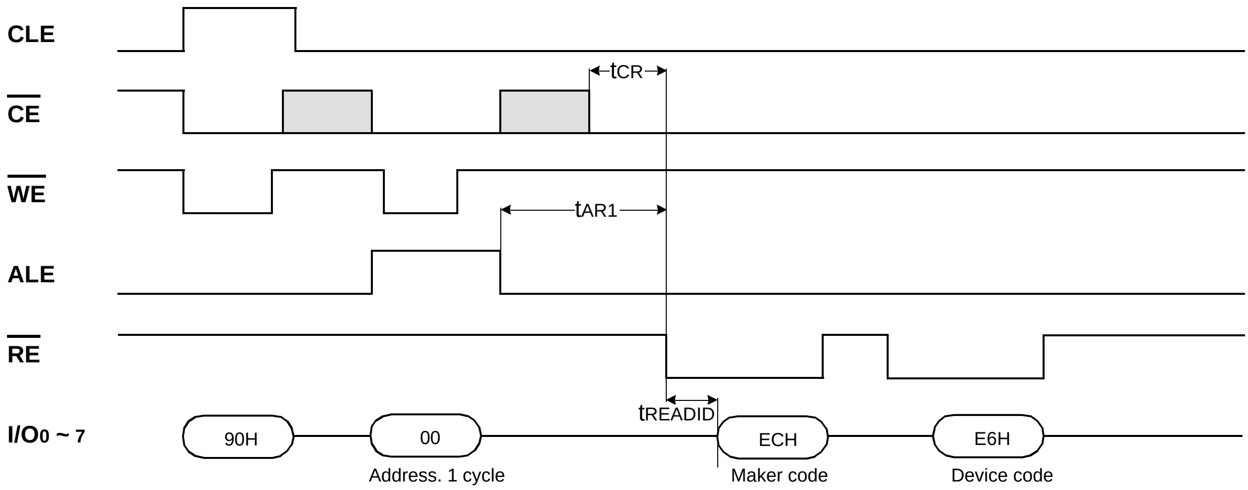
Table2. Status Register Definition

SR	Status	Definition
I/O_0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O_1	Reserved for Future Use	"0"
I/O_2		"0"
I/O_3		"0"
I/O_4		"0"
I/O_5		"0"
I/O_6	Device Operation	"0" : Busy "1" : Ready
I/O_7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90H to the command register, followed by an address input of 00H. Two read cycles sequentially output the manufacture code(ECH), and the device code (E6H) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 9 shows the operation sequence.

Figure 9. Read ID Operation



RESET

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70H command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE dose not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00H or 50H) should be given before sequential page read cycle.

Figure 10. RESET Operation

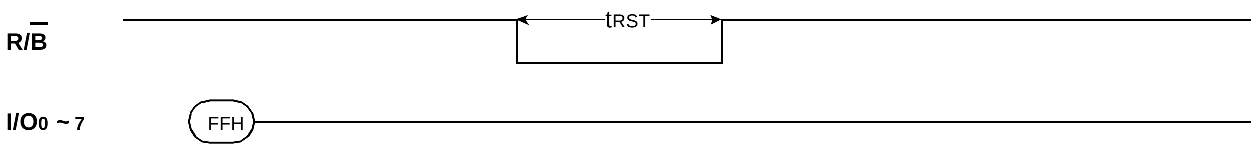
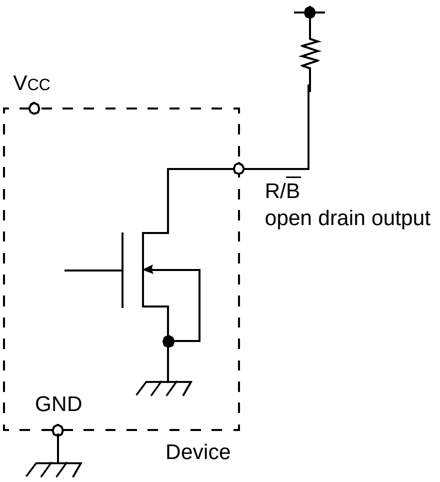


Table3. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{\text{BUSY}}$

The device has a R/$\overline{\text{B}}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{\text{B}}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{\text{B}}$ outputs to be Or-tied. An appropriate pull-up resister is required for proper operation and the value may be calculated by the following equation.



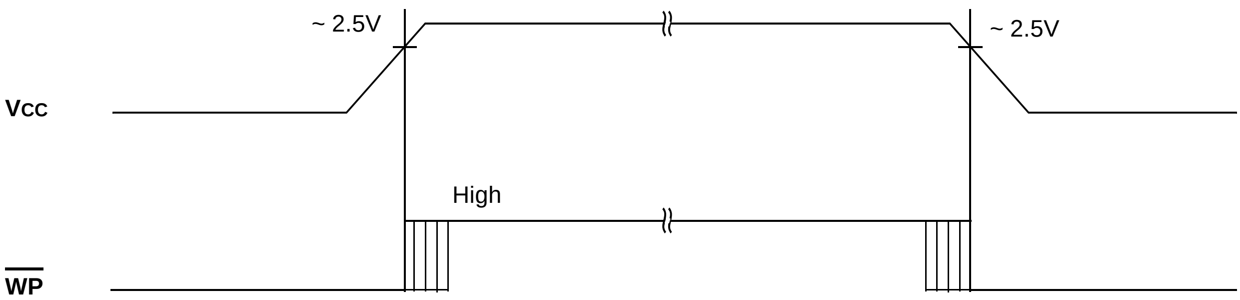
$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{\text{B}}$ pin.

DATA PROTECTION

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. $\overline{\text{WP}}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down as shown in Figure 11. The two step command sequence for program/erase provides additional software protection.

Figure 11. AC Waveforms for Power Transition



PACKAGE DIMENSIONS

44(40) LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)